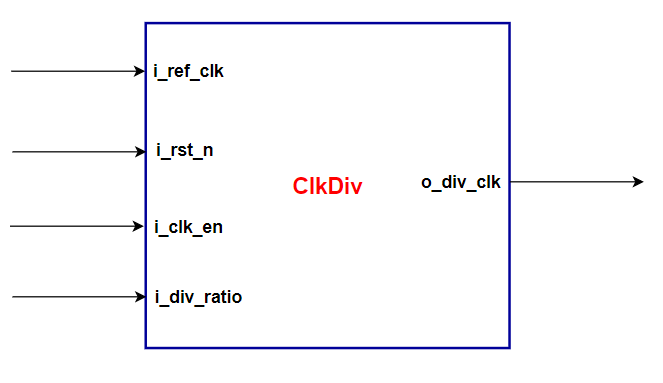
**Clock Divider**

**Introduction: -**

A clock divider is a circuit that takes an input signal of a frequency **fin** and generates an output signal of a frequency **fout**, where

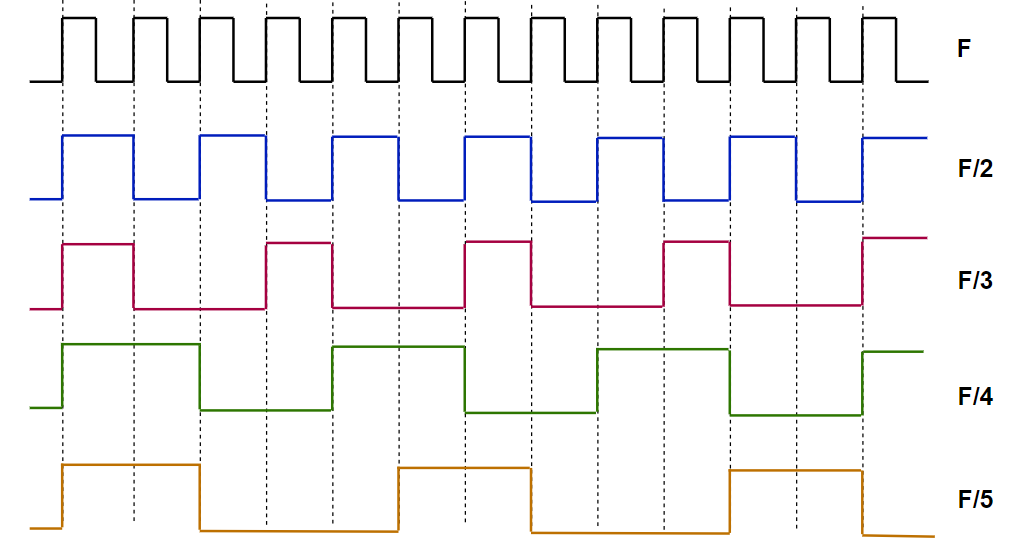
**fout = fin / n** and ''n'' is an integer

**Block Interface**



**Ports Description**

|  |  |  |
| --- | --- | --- |
| Width | Description | Signal Name |
| 1 | Reference Frequency | I\_ref\_clk |
| 1 | Active Low Asynchronous Reset | I\_rst\_n |
| 1 | Clock Divider Block Enable | I\_clk\_en |
| 1 | The divided ratio (integer value) | I\_div\_ratio |

**Waveforms**

**Requirements: -**

1. Write a Verilog Code to capture the above specifications
2. Write a testbench to test generation of different frequencies of both odd and even divided ratio of the reference frequency